AMENDMENT TO THE CLAIMS

Please amend the claims with the following complete listing of claims:

Claims 1- 19 (*Canceled*).

Claim 20. (*New*) A test structure for verifying an isolation trench etching in an SOI wafer, wherein the test structure in the SOI device comprises, after etching of isolation trenches, a row of islands, each of which is surrounded by a trench, said trenches having increasing trench width from one island to a next island and including a certain trench width of another isolation trench of an active circuit away from the test structure;

wherein a portion of the surrounding trench (a, b) of each island shares a common portion with the surrounding trench of the adjacent island;

wherein the respective common portion - except for an island having a broadest (e) or a narrowest (a) isolation trench - has the width of the adjacent surrounding trench having a next larger or a next smaller measure of width in the row.

Claim 21. (*New*) A method of verifying insulation trench etchings or isolation trench etchings in SOI substrates, the method comprising:

forming a test structure comprising a row of successive islands during an etch process or preparing the test structure for an etch process and measuring an electric pass several times during or after said trench etching;

wherein a plurality of measurements of the electric pass are performed to provide a plurality of measurement values;

wherein one of the measurements is performed between two adjacent first islands (A, B), a further measurement is performed between a different set of adjacent islands (B, C);

using the measurement values of said plurality of measurements for assessing a sufficient or appropriate depth of etched insulation trenches or isolation trenches located outside said test structure in an area of an active circuit in the SOI substrate.

Claim 22. (*New*) A method for verifying an insulation trench etching in an SOI substrate, comprising:

preparing a test structure (A, B, D, E) above a substrate of the SOI substrate and forming the test structure during a trench etching, measuring after or during said trench etching an electric pass between islands of the test structure, or between an island (A, B) and a substrate region (S) at least partially surrounding said island of the test structure; and

using the measurement results for assessing or detecting an appropriate depth of etched trenches located outside said test structure but being formed during said trench etching.

Claim 23. (*New*) The method of claim 21, wherein said test structure comprises, after etching of isolation trenches, a row of associated islands, each of which is surrounded by an isolation trench, said trenches having increasing width from island to island and including one isolation trench having a width corresponding to a width of an isolation trench associated to an active circuit;

wherein a portion of the surrounding trench (a, b) of each first island (A,B) has a common portion with a surrounding trench of an island located adjacent to said first island;

wherein the common portion has a width being the larger width of the widths of both concerned surrounding trenches.

Claim 24. (*New*) The method of claim 21, wherein said electric pass is a resistance or a conductance.

Claim 25. (*New*) The method of claim 21, wherein said electric pass is a current at a constant voltage or a voltage at a constant current.

Claim 26. (*New*) The method of claim 21, wherein the measurements are performed during the etching as etch process, and wherein the etch process is interrupted to perform a measurement between the islands or between an island and a surrounding crystal region.

Claim 27. (*New*) The method of claim 26, wherein the etching as etch process is continued when the measurement for a certain trench in the test structure having a certain width (d) corresponding to a width of a trench in the active circuit indicates that the certain trench is not completely etched through to the insulating layer of the SOI substrate.

Claim 28. (*New*) The method of claim 26, wherein the etching is stopped, when a trench surrounding an island of the test structure and having a width (d) corresponding to an isolation trench in the active circuit is etched through to the insulating layer, as determined by at least two measurements.

Claim 29. (*New*) A method for verifying insulation trench etchings in SOI wafers, wherein as active circuits dedicated devices or complete circuit modules are laterally dielectrically isolated by enclosing insulation trenches to form specific regions and a surrounding crystal region;

wherein a test structure is prepared on said SOI wafer for allowing a verification of at least one electric pass during a process step of insulation trench etching, the electric pass verification applied between at least one of :

specific regions (A,B; B,C) of the test structure; and

a specific region of the test structure and the surrounding crystal region (S);

the method further comprising:

preparing the test structure on the SOI wafer, said test structure having a row of functionally associated test islands after the trench etching process as said specific regions, each island being surrounded by a trench having a different width at least between respective two of said test islands;

wherein a relevant width of an insulation trench provided in the active circuits is positioned approximately in a central location within said row of test islands;

after the etch process, assessing a proper etch process result by repeatedly measuring an electric pass between respective two adjacent islands or between a respective island and the surrounding region (S) of said respective island;

using detected measurement values of the measurings as a measure or a test for a target depth as predefined depth of etched isolation trenches in the active circuits.

Claim 30. (*New*) The method of claim 29, wherein the width of each trench surrounding a respective island in the row of test islands increases in a step-wise manner from island to island.

Claim 31. (*New*) The method of claim 29, wherein the width of the insulation trench provided for the active circuits is a predefined value as a relevant insulation trench width.

Claim 32. (*New*) The method of claim 31, wherein, during successive verifications, it is started with an island having a surrounding trench width at least substantially corresponding to the relevant insulation trench width.

Claim 33. (*New*) The method of claim 31, wherein the step of assessing is completed after at least two measurements, when an abrupt change of a pass value is obtained, and when measuring an adjacent pair of islands having smaller trench width does not exhibit said abrupt change.

Claim 34. (*New*) The method of claim 21, wherein at least three, five, or more island regions are rowed up and functionally associated with each other.

Claim 35. (*New*) The method of claim 22, wherein at least three, five, or more island regions are rowed up and functionally associated with each other.

Claim 36. (*New*) The method of claim 29, wherein at least three, five, or more island regions are rowed up and functionally associated with each other.

Claim 37. (*New*) The method of claim 33, wherein not more than n-1 measurements are performed for n islands, wherein n being the number of islands in said row.

Claim 38. (*New*) The method of claim 22, wherein a maximum number of measurements corresponds to the number of islands in the test structure.

Claim 39. (*New*) The method of claim 21, wherein after the etch process the measurement values are evaluated, and wherein further etch processes of following SOI wafers are adapted to a result of the evaluation with respect to a targeted etch time.

Claim 40. (*New*) The method of claim 29, wherein the step of preparing is performed by a predetermined mask for etching a row of test islands.

Claim 41. (*New*) The method of claim 22, wherein said test structure comprises, after etching of isolation trenches, a row of associated islands, each of which is surrounded by an isolation trench, said trenches having increasing width from island to island and including one isolation trench having a width corresponding to a width of an isolation trench associated to an active circuit;

wherein a portion of the surrounding trench of each first island has a common portion with a surrounding trench of an island located adjacent to said first island;

wherein the common portion has a width being the larger width of the widths of both concerned surrounding trenches.

Claim 42. (*New*) The method of claim 22, wherein said electric pass is a resistance or a conductance.

Claim 43. (*New*) The method of claim 22, wherein said electric pass is a current at a constant voltage or a voltage at a constant current.

Claim 44. (*New*) The method of claim 22, wherein the measurements are performed during the etching as etch process, and wherein the etch process is interrupted to perform a measurement between the islands or between an island and a surrounding crystal region.

Claim 45. (*New*) The method of claim 44, wherein the etching as etch process is continued when the measurement for a certain trench in the test structure having a certain width corresponding to a width of a trench in an active circuit indicates that the certain trench is not completely etched through to the insulating layer of the SOI substrate.

Claim 46. (*New*) The method of claim 44, wherein the etching is stopped, when a trench surrounding an island of the test structure and having a width corresponding to an isolation trench in an active circuit is etched through to the insulating layer, as determined by at least two measurements.